Different strategies boost DSPs’ abilities

By Garrick Blalock
DSP Engineer
Berkeley Design Technology Inc.
Fremont, Calif.

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urred by the voracious number-crunching requirements of such popular DSP applications as digital wireless communication, the demand for high-performance DSP processors has never been greater. According to DSP market-research firm Forward Concepts, annual sales of programmable DSP processors will exceed $3 billion in 1997. DSP processor vendors have raced to meet this demand with new processors promising state-of-the-art performance. Not wanting to miss the boat, vendors of general-purpose processors have added DSP capabilities to their products and advocate using a single chip for both DSP and general processing. System designers have never faced as many options for implementing high-performance DSP.

Today’s processors use a variety of strategies to increase their DSP performance, including single-instruction, multiple-data (SIMD) instructions, multi-issue architectures, control and signal-processing architecture integration, and refinements on traditional DSP architectures.

SIMD instructions partition registers and ALUs so that multiple items of data are present in one register or memory location and can be processed in parallel by one instruction. For example, a SIMD processor might have a 64-bit register that can be partitioned into eight 8-bit data elements, four 16-bit data elements, or two 32-bit data elements or one 64-bit data element. Typically, a SIMD processor performs the same operation, such as addition or multiplication, on multiple pairs of data elements using just one instruction. SIMD instructions are commonly used to add DSP capabilities to 32- or 64-bit RISC/CISC architectures, since these processors already contain the wide buses and registers needed. However, SIMD techniques also can be used on dedicated DSP processors—Texas Instruments’ TMS320CXX, for example.

One highly publicized general-purpose processor to use SIMD instructions for DSP is the Intel Pentium processor. The first Pentium processor to include the MMX multimedia extensions. One MMX instruction operating on two 64-bit data registers partitioned into 16-bit data elements can multiply four pairs of multiplands, add the 32-bit products in pairs and save the two 32-bit sums in one 64-bit register with throughput of one instruction cycle. These types of operations are very useful for calculating vector dot products and complex number multiplications.

Sun Microelectronics has also developed SIMD multimedia extensions for its UltraSPARC architecture. Like the MMX extensions, Sun’s Visual Instruction Set (VJS) allows 64-bit registers to be partitioned into 8-, 16- or 32-bit data elements that can be manipulated in parallel.

One of the attractions of SIMD instructions is the ability to select an appropriate data word length. If precision is needed, programmers can use 16-bit data elements and operate on four elements in parallel, for example. Alternatively, if more precision is needed, the programmer can choose 32-bit elements at the price of performing fewer operations in parallel.

If SIMD instructions use fixed-point arithmetic, parallel processing can be accomplished by simply partitioning an existing data path. For example, if a processor contains a 32-by-32 64-bit multiplier, the multiplier could be dissected into four 8-by-8 16-bit multipliers that operate in parallel. Unfortunately, realizing SIMD instructions’ performance potential often requires restructuring algorithms so that elements can be processed simultaneously. This requirement can make optimizing code for SIMD instructions very difficult and some applications may not see significant improvement with SIMD instructions. For example, application with sequential data dependencies, such as adaptive filtering, may be limited in how many calculations can be done in parallel. In many DSP applications, however, SIMD instructions are very effective.

Multi-issue architectures can execute several different instructions with sequential data dependencies, such as adaptive filtering, may be limited in how many calculations can be done in parallel. In many DSP applications, however, SIMD instructions are very effective.

System designers never had so many options for implementing the high-performance digital signal processor.

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The MMX Pentium can issue up to two SIMD instructions in parallel. With both SIMD instructions and multi-issue architectures, taking full advantage of the parallel-execution abilities of processors typically requires careful programming and advanced tools that are often unavailable. This concern is especially relevant to general-purpose processors, which often lack cycle-accurate simulators and other tools needed to develop efficient DSP code.

Texas Instruments has introduced the TMS320C62XX family of DSP processors. The C62XX family comprises the first dedicated DSP processors to take advantage of a VLIW-like architecture, and thus promises substantial performance.

Unlike the dynamic instruction grouping used by superscalar general-purpose processors, grouping on the C62XX is done by the programmer or the compiler. The C62XX fetches eight instructions at a time and, based on a bit in each instruction, executes between one and eight of the instructions. This form of static instruction scheduling greatly simplifies predicting code-execution time, but shifts the burden of instruction grouping to the programmer and code-development tools. In the best-case scenario, the C62XX can perform four arithmetic operations, two multiplications and two address calculations in one instruction cycle.

Vendors of processors with traditional DSP architectures have not stood still. For example, Motorola has recently refined its 24-bit fixed-point DSP5600X family of processors to develop the new DSP563XX. The most notable change is the addition of a deeper pipeline that increases the instruction-execution throughput to about twice that of the DSP5600X. Motorola also added special instructions, such as bit-manipulation instructions and conditional execution instructions, that speed the processing of many DSP applications.

The DSP563XX also supports a coprocessor interface that has allowed Motorola to add hardware optimized for key DSP algorithms, such as Viterbi decoding, which is heavily used in wireless communications. Like many DSPs, the DSP563XX features peripherals designed to increase the processor’s efficiency in DSP applications. For example, to reduce the number of instructions needed for high-bandwidth I/O, a six-channel direct-memory-access (DMA) controller allows transfers of data between any combination of internal or external memory locations without the CPU’s intervention.

Other vendors also are improving their DSP processors. Analog Devices has introduced the ADSP-2106X, a new family of fixed-point 16-bit processors based on the ADSP-210XX family. The ADSP-210XX extends the ADSP-210XX’s pipeline from two to three stages, allowing the processor to run at faster clock speeds. By optimizing the instruction set, the ADSP-210XX instruction set is more orthogonal than the ADSP-210XX instruction set. Furthermore, performing algorithms on two unrelated data streams has been facilitated by the extensive use of context-switched shadow registers. These shadow registers help reduce the code complexity and MIPS-usage associated with switching between interrupts, core-processing tasks and multiple data sets.

Lattice Technologies has refined its 16-bit fixed-point 1616X family to run at 120 MHz, the fastest instruction-excitation rate of any programmable DSP currently in mass production. Lattice has also pushed the 16XX-family operating voltage down to a 1.2-V nominal on some family members. In contrast to many general-purpose processors, which consume far too much power for portable applications like cellular telephones, members of the DSP16xx family can consume as little as 40 mW at 60 MHz.

Traditional dedicated DSPs offer many advantages. Because DSP processor instruction sets and peripherals are targeted specifically at signal processing, they typically offer very competitive price/performance ratios, especially in applications that can use fixed-point arithmetic. Unlike general-purpose processors, DSPs typically have signal...

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Digital Signal Processing

Different strategies can increase DSP performance

An interesting counterpoint to microcontrollers with DSP enhancements such as Hitachi’s SH-DSP is Motorola’s recently announced DSP560XX family. The DSP560XX provides architectural and I/O features to address the needs of microcontroller applications.

The execution time for some of the processors discussed above can be found in Berkeley Design Technology’s (BDT) FFT benchmark, one of 11 benchmarks in the BDT Benchmark suite research reports. DSP on General-Purpose Processors and Buyer’s Guide to DSP Processors. The reports also contain results for a variety of DSP functions, cost/performance and memory usage, as well as more detailed analysis of each processor.

The best approach to high-performance signal processing depends strongly on the application. In PC applications, for example, in a cellular telephone, the DSP is likely to handle speech coding and baseband functions while a microcontroller handles the user/machine interface and other control processing. The incentive to merge these two processors is great: lower power consumption, fewer programming models to learn, etc.

Dual controls

Integrating a dedicated DSP data path with a microcontroller architecture creates processor well-suited for both signal processing and system control. For example, the Hitachi SH-DSP adds a complete fixed-point DSP data path and instruction set to Hitachi’s successful SH-2 microcontroller architecture. This unusual hybrid approach allows programmers to add DSP functionality while protecting their investment in SH-2 code, which runs unaltered on the SH-DSP. Programmers can access the SH-DSP’s DSP data path by simply adding DSP instructions to a SH-2 program. The SH-DSP fetches instructions sequentially and issues DSP and microcontroller instructions to the appropriate execution unit.

Because hybrid architectures like the SH-DSP are partitioned into a dedicated DSP data path and a microcontroller data path, both system control and signal processing can be implemented efficiently. However, the presence of two separate instruction sets can complicate programming, and interactions between the two data paths can sometimes hinder performance.

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Processors intended for portable applications will consume less power with the help of better power-management features and lower operating voltages. DSP-device designers will continue to improve their architectures' suitability for compiled code, reducing the amount of code that must be tediously written in assembly language. Likewise, processor vendors and third-party companies will improve their software design tools, although tool improvements often lag the increasing complexity of processors. Finally, as semiconductor-fabrication technologies progress, processor operating speeds will undoubtedly increase.

Landscape shifting for DSP design

RISC processors have traditionally been programmed in high-level languages such as C; the performance-driven DSPs traditionally were handled in assembly language. Though still generally true for fixed-point DSPs, which now can handle algebraic assembly language to ameliorate the ease-of-use issue, floating-point DSPs are now more efficiently programmed in high-level languages.

In each of these areas, RISC and DSP architectures remain wide apart. As prices and functionality become similar in the future, designers will be forced to consider whether their products will be used in the real-time environments where DSPs will continue to excel.

As DSP performance reaches 1,500 MIPs in the years ahead, the performance rift between RISC and DSP will widen. DSPs are more efficient for real-time signal processing and will continue to be so.